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10/043,237

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FILE 'WPIX, INPADOC, JAPIO, PATOSEP, PATOSWO' ENTERED AT 09:44:44 ON 25
JUN 2003

L1 E JP2001-214613/AP,PRN
 4 S E3-E4

L1 ANSWER 1 OF 4 WPIX (C) 2003 THOMSON DERWENT
 AN 2003-330435 [31] WPIX
 DNN N2003-264542 DNC C2003-085761
 TI MOSFET manufacturing method involves using mask of desired width to defined gate length to implant ion in substrate for forming pocket regions.
 DC L03 U11 U12
 IN DOUMAE, Y
 PA (OKID) OKI ELECTRIC IND CO LTD; (DOUM-I) DOUMAE Y
 CYC 2
 PI US 2003013243 A1 20030116 (200331)* 12p
 JP 2003031801 A 20030131 (200331) 8p
 ADT US 2003013243 A1 US 2002-43237 20020114; JP 2003031801 A JP 2001-214613 20010716
 PRAI JP 2001-214613 20010716
 AB US2003013243 A UPAB: 20030516
 NOVELTY - A conductive layer is formed on the main surface of a semiconductor substrate (10). A gate electrode is formed by etching the conductive layer, using a mask which has a desired width to defined gate length. The source and drain regions are formed in the main surface. Multiple pocket regions are formed in the substrate by implanting ion in the substrate using the mask.
 USE - For manufacturing metal oxide semiconductor field effect transistor MOSFET.
 ADVANTAGE - Since the mask of desired width to defined gate length is used, the width of the gate electrode is increased along the downward direction to secure the predetermined gate length after ion implantation. The pocket region formed by the ion implantation below the gate electrode expand longer by the thickness of the conductive layer.
 Therefore the expansion of the depletion layer between the source and drain regions is inhibited efficiently. The FET is formed easily without producing any variation in the electrical characteristics, at a comparatively low impurity concentration.
 DESCRIPTION OF DRAWING(S) - The figure shows a cross sectional view illustrating the process of manufacturing FET.
 semiconductor substrate 10
 Dwg.1e/3

L1 ANSWER 2 OF 4 INPADOC COPYRIGHT 2003 EPO

LEVEL 1

AN 198851797 INPADOC ED 20030310 EW 200310 UP 20030520 UW 200320
 TI METHOD FOR MANUFACTURING FIELD-EFFECT TRANSISTOR
 IN DOMAE YASUHIRO
 INS DOMAE YASUHIRO
 PA OKI ELECTRIC IND CO LTD
 PAS OKI ELECTRIC IND CO LTD
 TL English
 DT Patent
 PIT JPA2 DOCUMENT LAID OPEN TO PUBLIC INSPECTION
 PI JP 2003031801 A2 20030131
 AI JP 2001-214613 A 20010716
 PRAI JP 2001-214613 A 20010716

L1 ANSWER 3 OF 4 INPADOC COPYRIGHT 2003 EPO

LEVEL 1

AN 195454055 INPADOC ED 20030210 EW 200306 UP 20030326 UW 200312
TI METHOD OF MANUFACTURING FIELD EFFECT TRANSISTOR
IN DOUMAE YASUHIRO
INS DOUMAE YASUHIRO
INA JP
PA DOUMAE YASUHIRO
PAS DOUMAE YASUHIRO
PAA JP
DT Patent
PIT USAA PATENT APPLICATION PUBLICATION (PRE-GRANT)
PI US 2003013243 AA 20030116
AI US 2002-43237 A 20020114
PRAI **JP 2001-214613** A **20010716**
OSCA 138:099439

AB A method for manufacturing a field effect transistor (FET) which is capable of effectively inhibiting an expansion of a depletion layer between a source and a drain in the FET, without causing variations in electrical characteristics, at a comparatively low impurity concentration. After a conductive layer for a gate electrode has been formed on a semiconductor substrate, in order to remove unwanted portions from the conductive layer by lithography, an etching mask is formed for the gate electrode and, by using the etching mask as a mask for ion implantation, an impurity is implanted to form an impurity region in a predetermined region of a semiconductor substrate existing under the conductive layer.

L1 ANSWER 4 OF 4 JAPIO COPYRIGHT 2003 JPO

AN 2003-031801 JAPIO

TI METHOD FOR MANUFACTURING FIELD-EFFECT TRANSISTOR

IN DOMAE YASUHIRO

PA OKI ELECTRIC IND CO LTD

PI JP 2003031801 A 20030131 Heisei

AI **JP 2001-214613** (JP2001214613 Heisei) 20010716

PRAI **JP 2001-214613**20010716

SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2003

AB PROBLEM TO BE SOLVED: To provide a method for manufacturing a field-effect transistor capable of effectively suppressing extension of a depletion layer between the source and drain without causing dispersion of electrical characteristic but with a comparative low impurity density. SOLUTION: After forming a conductive layer 14 for the gate electrode on a semiconductor substrate 10, an etching mask 15 is formed for the gate electrode on the conductive layer to remove the unnecessary part by photolithography. With the etching mask ion implantation, impurity for forming an impurity area 17 is implanted into the prescribed area of the semiconductor substrate under the conductive layer by ion implantation. COPYRIGHT: (C)2003,JPO

LEVEL 1

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TI METHOD OF MANUFACTURING FIELD EFFECT TRANSISTOR
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INA JP
PA DOUMAE YASUHIRO
PAS DOUMAE YASUHIRO
PAA JP
DT Patent
PIT USAA PATENT APPLICATION PUBLICATION (PRE-GRANT)
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AI US 2002-43237 A 20020114
PRAI JP 2001-214613 A 20010716
OSCA 138:099439
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L1 ANSWER 4 OF 4 JAPIO COPYRIGHT 2003 JPO
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PI JP 2003031801 A 20030131 Heisei
AI JP 2001-214613 (JP2001214613 Heisei) 20010716
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